Circuit arrangement for generating clock pulses in a
communication system

The invention relates to a circuit arrangement for
5   generating clock pulses in a communication system as
claimed in the preamble of claim 1.

In ISDN (Integrated Services Digital Network), the
connection at the subscriber end, the so-called ISDN
10   basic access, have a number of reference points R, S,
T, U which correspond to interfaces.

Figure 1 shows a model of the ISDN basic access with a
connection to an exchange. The U interface forms the
15   line termination both at the subscriber end and at the
exchange end.

The exchange have a local line termination 2 (LT) and a
digital ISDN exchange termination 1 (ET) which
20   communicate with one another via the V interface.

The ISDN basic access have a network termination 3 (NT)
at the subscriber end. The network termination 3 is
composed of a first network termination 7 (NT-1), which
25   transfers user information and signaling information to
the exchange (physical network termination according to
level 1 of the ISO/OSI reference model), and a second
network termination 8 (NT-2) which handles
concentrating and switching tasks (logical network
30   termination according to level 2 and 3 of the ISO/OSI
reference model). The first and second network
terminations 7, 8 are connected via the T interface.

A digital ISDN-compatible subscriber terminal 4 (TE1)
35   can be connected directly to the second network
termination 8 via the S interface.

To connect an analog subscriber terminal 6 (TE2), a terminal adapter 5 (TA) is necessary which is connected to the second network termination 8. The analog subscriber terminal 6 can then be connected to the

5   terminal adapter 5 via the R interface.

In the ISDN basic access, hierarchical clock synchronization is used: a device configured as master, for example a device executing the top levels of the

10   ISO/OSI reference model, synchronizes a device configured as slave, for example a device executing the lower levels of the ISO/OSI reference model.

In figure 1, the exchange 2 is configured as master of

15   the network termination 3 and synchronizes it.

In the case of a multiplicity of slaves which are synchronized by a master, one of these slaves is appointed as reference clock generator for the

20   remaining slaves. In the case of a failure of the reference clock generator, a further slave is appointed as reference clock generator and so forth.

Figure 2a shows an arrangement in which, at the

25   subscriber end in an ISDN basic access, a number of first network terminations 12 to 14 are connected to a telecommunication system 15 via a common network termination system bus 18. The telecommunication system 15 have the further elements of the ISDN basic access

30   of the subscriber end. A number of subscriber terminals 16 to 17 can be connected to the telecommunication system 15. The first network terminations 12 to 14 are in each case connected to local exchange terminations 9 to 11 via a U interface.

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For the hierarchical clock synchronization, the first network terminations 12 to 14 execute tasks of the same

level of the ISO/OSI reference model so that one of the
first network terminations 12 to 14 or, respectively,
one of the corresponding U interfaces must be selected
as first reference clock generator for the remaining
first network terminations or, respectively, U
interfaces. Furthermore, further reference clock
generators must be determined which take over the task
of the first reference clock generator in the event of
its failure. The network termination system bus 18 must
be synchronized to the respective reference clock
generator.

Figure 2b shows in detail the clock generation and
distribution of various clocks in the arrangement
pictured in figure 2a. The clocks necessary for
operating the arrangement are generated via a phase
locked loop 100 and a clock divider 101. To illustrate
the direction of synchronization, a line termination 16
(LT) of the network operator, which is responsible for
the synchronization, is shown diagrammatically on the
right-hand side in figure 2b. Furthermore, a network
termination with subscriber terminal NT/TE 17 is shown
by way of example on the left-hand side.

Each of the first network terminations 12 to 14 have
its own 15.36 MHz crystal by means of which, for
example, a 512 kHz clock CLS is generated as reference
clock. The clock CLS is supplied to the phase locked
loop 100 which, in turn, generates from the 512 kHz
clock a 15.36 MHz clock XIN, an 8 kHz frame clock FSC
and a bit clock DCL which has a frequency of between
512 and 4096 kHz. The frame clock FSC and the bit clock
DCL are supplied to each of the first network
terminations 12 to 14 and each of the local exchange
terminations 9 to 11 via in each case one line. The
clock XIN is fed back to the phase locked loop 100 via
the clock divider 101 and supplied in parallel to the

local exchange terminations 9 to 11 via one line. In this arrangement, the reference clock generator is the 512 kHz clock CLS which is generated in each of the first network terminations 12 to 14.

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Figure 3 shows an arrangement in which a line termination 20 which is not ISDN capable provides subscribers with access to the public ISDN network by means of a digital loop carrier (DLC) system.

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For this purpose, a number of first subscriber accesses 35 are combined in a first so-called "D-channel bank" 22 in a digital ISDN exchange termination 19. The basic channels of each basic access are transmitted

15 concentrated to the line termination 20 via a first broadband transmission channel 23.

In the line termination 20, the basic channels of a second "D-channel bank" 24 are distributed to the

20 corresponding subscriber accesses 25 to 32 which are also called line cards in technical language. A number of accesses 25 to 28 are then combined in a third "D-channel bank" 21 to form so-called "central office terminals" and are transmitted via a second broadband

25 transmission channel 33 to a subscriber having a number of network terminations 36 to 37.

The individual accesses 25 to 28 are there distributed to the corresponding network terminations via a fourth

30 "D-channel bank" 34 which forms the so-called remote digital terminal (RDT).

The arrangements shown in figures 2 to 3 can also be used for so-called xDSL (x Digital Subscriber Line)

35 systems such as ADSL, SDSL, VDSL or HDSL. It is only necessary to replace the ISDN transmission method at the U interfaces by the corresponding xDSL transmission

method. The basic arrangement shown in figures 2 to 3 will not change.

In the arrangement shown in figure 3, similarly to the arrangement shown in figure 2, a reference clock generator must be selected and other reference clock generators used as replacement in the event of a failure of the first reference clock generator must be determined for the hierarchical clock synchronization.

The invention is, therefore, based on the object of creating a circuit arrangement for generating clock pulses in a communication system which, in particular, is based on ISDN or xDSL, in which the disadvantages described initially are avoided and, in particular, the circuit arrangement can be connected directly to a telecommunication system or a concentrator via a common network termination system bus.

This object is achieved by a circuit arrangement having the features of claim 1. Preferred embodiments of the invention are the subject matter of the dependent claims.

The circuit arrangement for generating clock pulses in a communication system according to the invention have at least one network termination, where each network termination can be connected to at least one transmission line in each case and to a bus and where a clock is provided for synchronizing the bus. A multiplicity of clock generators for generating the clock and means for selecting a clock generator are provided in the circuit arrangement. The circuit arrangement can be advantageously connected to a telecommunication system via the bus without any additional circuit expenditure.

The means for selecting a clock generator are preferably programmable. Furthermore, the means for selecting a clock generator can be programmable via a register. Due to the programming, the circuit arrangement can be adapted to various requirements and, in particular, in the event of a failure of one of the clock generators, is still operational by means of simple reprogramming.

The means for selecting a clock generator preferably has a first multiplexer, to whose inputs transmission lines can be connected, particularly via so-called phase control units, and a signal from which a clock is derived is received via one of the transmission lines. In other words, the received signals of the connected transmission lines are used as clock generator, as it were, and the phase control units extract the clock information from the signal received in each case. In particular, the means for selecting a clock generator has a second multiplexer, at the inputs of which the output signal of a phase locked loop and a reference clock are present. The phase locked loop is preferably supplied with a further clock from a crystal oscillator circuit and the output signal of the first multiplexer as input signals.

In a preferred embodiment, the following three clock generators can be used as reference clock generators: a signal received via one of the transmission lines is used as first clock generator, the reference clock itself is used as second clock generator if all transmission lines are in active, and the combination of received signals from at least two transmission lines is used as third clock generator, the clock generated by the third clock generator being generated, in particular, by averaging the clock information determined from the signals of the transmission lines

involved. The averaging for determining the clock can also be provided with weighting. The signals of all four transmission lines are preferably combined in order to derive the clock information for the reference

5   clock.

The signals which are transmitted via the transmission lines preferably correspond to the U interface protocol of ISDN. The circuit arrangement can then be

10 advantageously used in ISDN applications in which a number of U interfaces are administered.

On the other hand, the signals which are transmitted via the transmission lines can also correspond to an

15 XDSL protocol. For this purpose it is only necessary to change the signal transmission method to an XDSL transmission method. In particular, the XDSL protocol can correspond to an ADSL or SDSL or VDSL or HDSL protocol.

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Preferred embodiments of the invention are found in the subsequent description in conjunction with the drawings, in which:

25 Figure 1 shows a model of the ISDN basic access with a connection to an exchange,

Figure 2a shows an arrangement in which at the subscriber end in an ISDN basic access, a number of

30 first network terminations are connected to a telecommunication system via a common network termination system bus,

Figure 2b shows the clock generation and distribution

35 in the arrangement shown in figure 2a,

Figure 3 shows an arrangement in which a line

termination provides subscribers with access to the public ISDN network by means of a digital loop carrier (DLC) system,

5   Figure 4 shows a first exemplary embodiment of a circuit arrangement according to the invention, and

Figure 5 shows a second exemplary embodiment of a circuit arrangement according to the invention.

10   Figures 1 to 3 which relate to the prior art have already been discussed in the introduction to this description.

15   Figure 4 shows an integrated circuit 40 which have four U interfaces 41 to 44. The integrated circuit 40 is used in a communication system for connecting four U interfaces to a common network termination system bus which, in turn, can be connected to a telecommunication
20   system.

An external reference clock 46 which is generated, for example, by another integrated circuit, can be fed into the integrated circuit 40. This external reference
25   clock 46 is needed when none of the four U interfaces are active and accordingly no U interface is available as reference clock generator.

Each of the four U interfaces 41 to 44 can be
30   programmed as reference clock generator. For this purpose, the integrated circuit 40 have a first multiplexer 47 which can be controlled via a first control signal 45. To extract a clock signal from the respective received signals of the U interfaces 41, 42,
35   43, 44, the multiplexer 47 in each case have a phase control unit (PCU) 66, 67, 68, 69 for each input. The first control signal 45 switches one of the four U

interfaces 41 to 44, which are connected to the inputs
of the first multiplexer 47, through to the output of
the first multiplexer 47. The output signal of the
multiplexer 47 is conducted to a phase locked loop 48
5   which receives a clock of 15.36 MHz via a clock
generator 55. The 15.36 MHz clock is available as
output signal 54, for example for other integrated
circuits. The clock generator 55 can be connected to a
15.36 MHz crystal 58 via connections 56 and 57. From
10 the signals received via a U interface operating as
reference clock generator, the phase locked loop 48
regenerates the reference clock which is supplied to a
second multiplexer 49. The second multiplexer 49 is
switched by a second control signal 51. The second
15 multiplexer switches either the reference clock
regenerated from a U interface or the external
reference clock 46 fed in if none of the four U
interfaces are active, through to a PLL/clock divider
unit 50. The PLL/clock divider unit 50 divides a first
20 clock at its input into a second clock 52 and a third
clock 53. The second clock 52 can be used for
synchronizing a network termination system bus and have
an 8 kHz frame clock FSC. The third clock 53 have a bit
clock DCL. Furthermore, the PLL/clock divider unit 50
25 uses the clock generated by the clock generator 55.

The integrated circuit 40 can be programmed as master
or as slave. This makes it possible to set the
direction of synchronization of an arrangement in which
30 the integrated circuit 40 is used. In master mode, the
reference clock generator can be set to one of the
following clock sources by programming the integrated
circuit 40:
-   one of the four U interfaces 41 to 44 is used as
35 reference clock generator; or
-   the mean value over all four U interfaces 41 to 44
is formed; the mean value is then used as reference

clock generator; or

− an external reference clock 46 is used as reference clock generator; this setting is appropriate if none of the four U interfaces 41 to 44 are active.

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Figure 5 shows these three cases of operation.

A first 59, second 60 and third 61 integrated circuit as shown in figure 4 are interconnected to form a chain

10 and are used for driving a total of twelve U interfaces U1 to U12.

The first integrated circuit 59 is configured as master. For this purpose, a 15.36 MHz crystal 62 is

15 connected to the first integrated circuit 59. By this means, a 15.36 MHz clock is generated internally which is conducted as clock signal 62 to a connection XIN of the second integrated circuit 60 provided for connecting a crystal. As a result, the second

20 integrated circuit does not need a crystal. The U interfaces U1 to U4 connected to the first integrated circuit 59 are all inactive, i.e. no signal is transmitted or received via these interfaces. None of the U interfaces U1 to U4 can thus be used as reference

25 clock generator.

Of the U interfaces U5 to U8 connected to the second integrated circuit 60, U6 and U8 are active, i.e. a signal is transmitted or received via these two

30 interfaces. The second integrated circuit 60 is programmed in such a manner that U interface U8 is to be used as reference clock generator. For this purpose, the reference clock signal 64, which is generated internally in the second integrated circuit 60 via the

35 U interface U8, is conducted as external reference clock to the first integrated circuit 59, the master. The first integrated circuit 59 is programmed for an

external reference clock for this purpose.

The third integrated circuit 61 is supplied with the
15.36 MHz clock 63 at the terminal XIN provided for
5   connecting a crystal from the second integrated circuit
60. In this integrated circuit, too, a crystal is
saved. If at least one of the U interfaces U9 to U12
connected to the third integrated circuit 61 is active,
i.e. a signal is received or transmitted via one of the
10 U interfaces, the third integrated circuit is
programmed as standby reference clock generator for the
second integrated circuit 60. For this purpose, the
reference clock 65 is conducted to the second
integrated circuit 60 as external reference clock from
15 the third integrated circuit 61. The second integrated
circuit 60 and third integrated circuit 61 are
configured as slaves and accordingly receive the frame
clock FSC and the bit clock DCL from the first
integrated circuit 59.
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The second integrated circuit is programmed as
reference clock generator but can be reprogrammed to
the external reference clock from the third integrated
circuit 61 if all connected U interfaces U5 to U8 fail.
25 For this purpose, a circuit for monitoring the U
interfaces can be provided which automatically sets the
reference clock generator, i.e. reprograms the second
integrated circuit in this case.